

WHAT IS CLAIMED IS:

1. A bit stream processor, comprising:
a memory having one or more inputs for receiving variables, said variables defining a plurality of variable combinations;
5 an opcode input of said memory for inputting selected ones of one or more opcodes, each said variable combination associated with a unique said opcode; and
an output of said memory for outputting a bit stream.
2. The processor of Claim 1, wherein said memory is a bit-addressable memory where each said variable combination is mapped to a unique bit location in said memory.
3. The processor of Claim 1, wherein said memory comprises binary memory devices which can be individually and selectively read.
4. The processor of Claim 1, wherein said variable combinations comprise separate address inputs which are selected by said opcode.
5. The processor of Claim 1, wherein the processor generates said output bit stream as a function of Boolean operations performed on said variables.
6. The processor of Claim 1, wherein every variable combination at said inputs is defined by a unique opcode.
7. The processor of Claim 1, wherein each variable input accommodates is a single bit stream.

8. A method of bit stream processing, comprising the steps of:
providing a memory having one or more inputs for receiving variables, the
variables defining a plurality of variable combinations;
inputting selected ones of one or more opcodes into an input of the memory,
each variable combination associated with a unique opcode; and
outputting a bit stream from an output of the memory.
9. The method of Claim 8, wherein the memory in the step of providing is a bit-addressable memory where each variable combination is mapped to a unique bit location in the memory.
10. The method of Claim 8, wherein the memory in the step of providing comprises binary memory devices which can be individually and selectively read.
11. The method of Claim 8, wherein the variable combinations comprises separate address inputs which are selected by the opcode.
12. The method of Claim 8, wherein the processor generates the output bit stream as a function of Boolean operations performed on the variables.
13. The method of Claim 8, wherein every variable combination at the inputs is defined by a unique code.
14. The method of Claim 8, wherein each variable input accommodates a single bit stream.

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